

**S211**

**A Configurable System-on-Chip  
Device Facilitates Customization  
and Reuse**



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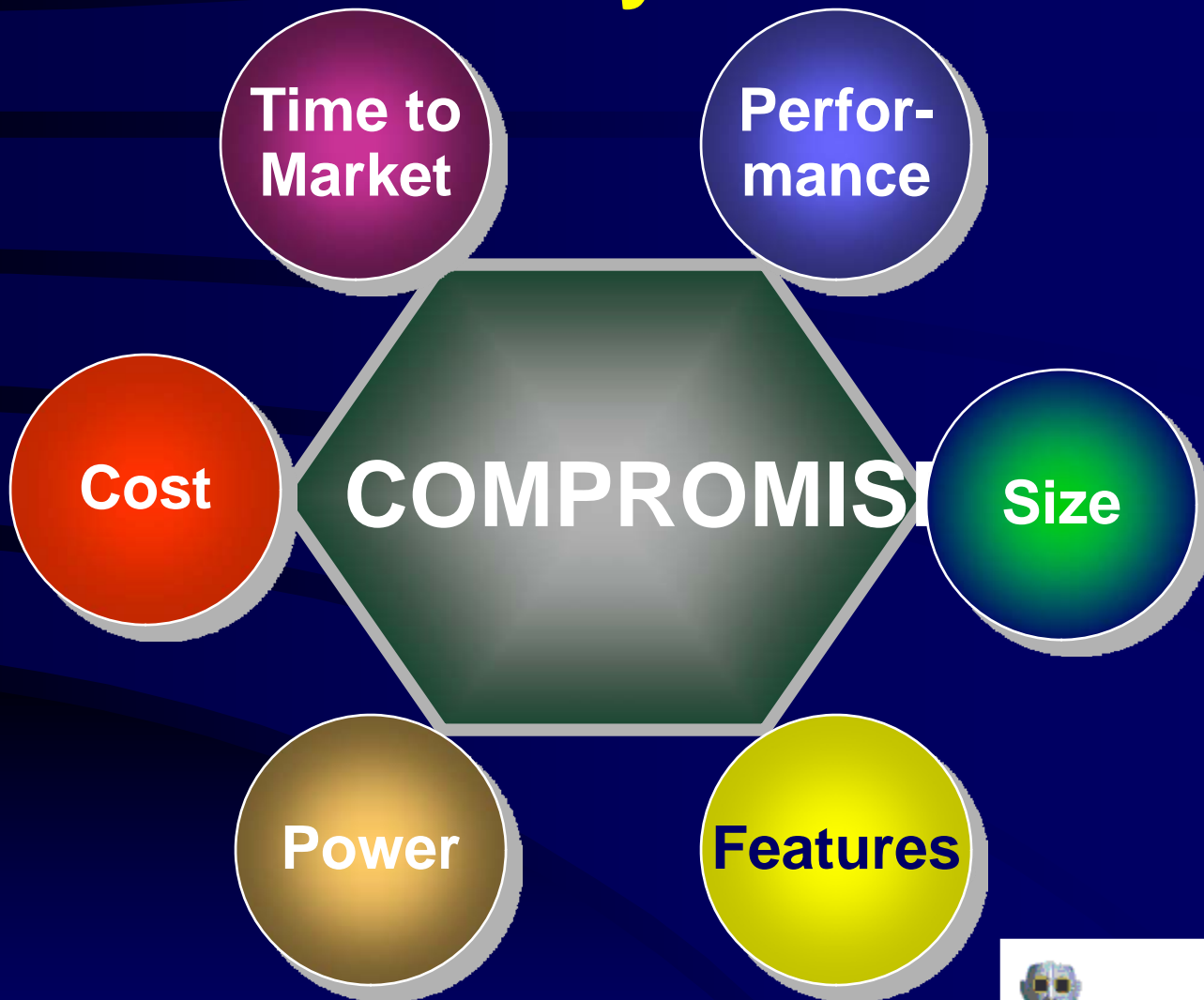
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# Agenda

- **Embedded System Challenges**
- **Industry Trends**
- **The Next Logical Step: A Configurable System-on-Chip**
- **Technical Challenges**
  - System communication, device structure
  - Debugging
  - Maintaining hardware/software design flows
- **Summary/Questions**

# The Embedded System Challenge

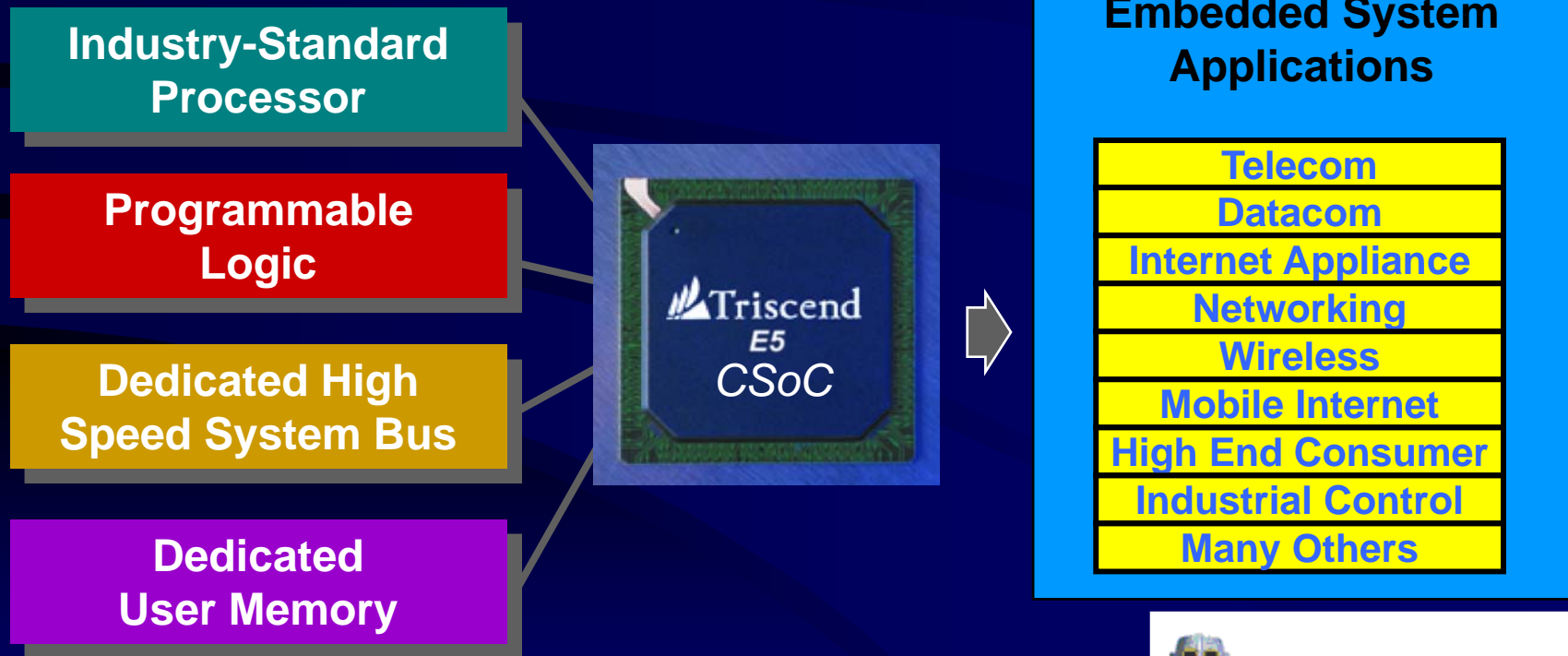


# Industry Trends

- **Advanced process technologies enable cost-effective system-on-a-chip designs and multi-million-gate FPGAs**
- **ASIC/FPGA densities now outstrip the capabilities to easily verify a design**
- **Adaptability is a desirable attribute**
- **Integrating system logic (memory, CPU) is expensive in FPGA logic**

# The Next Logical Step ...

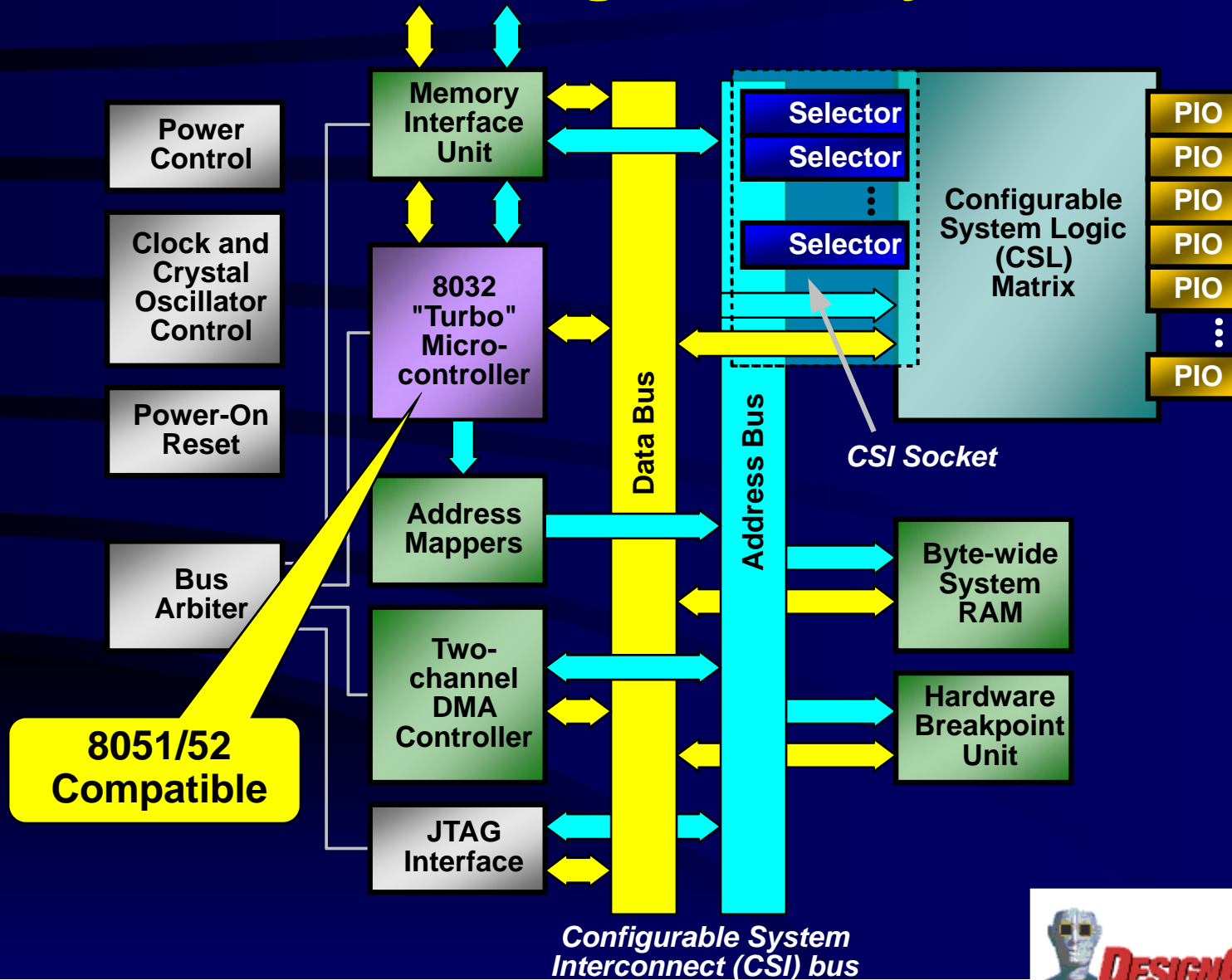
- **Configurable System-on-Chip (CSoC)**
  - Pre-verified processor sub-system
  - Embedded programmable logic



# Configurable System-on-Chip

- Pre-verified, configurable system integrated on a single chip
- Leverages standard logic design and processor development tools
- Leverages the design advantages of both processors and programmable logic
- Fast time-to-market for embedded systems
- System-on-a-chip for the masses

# Triscend E5 Configurable System-on-Chip

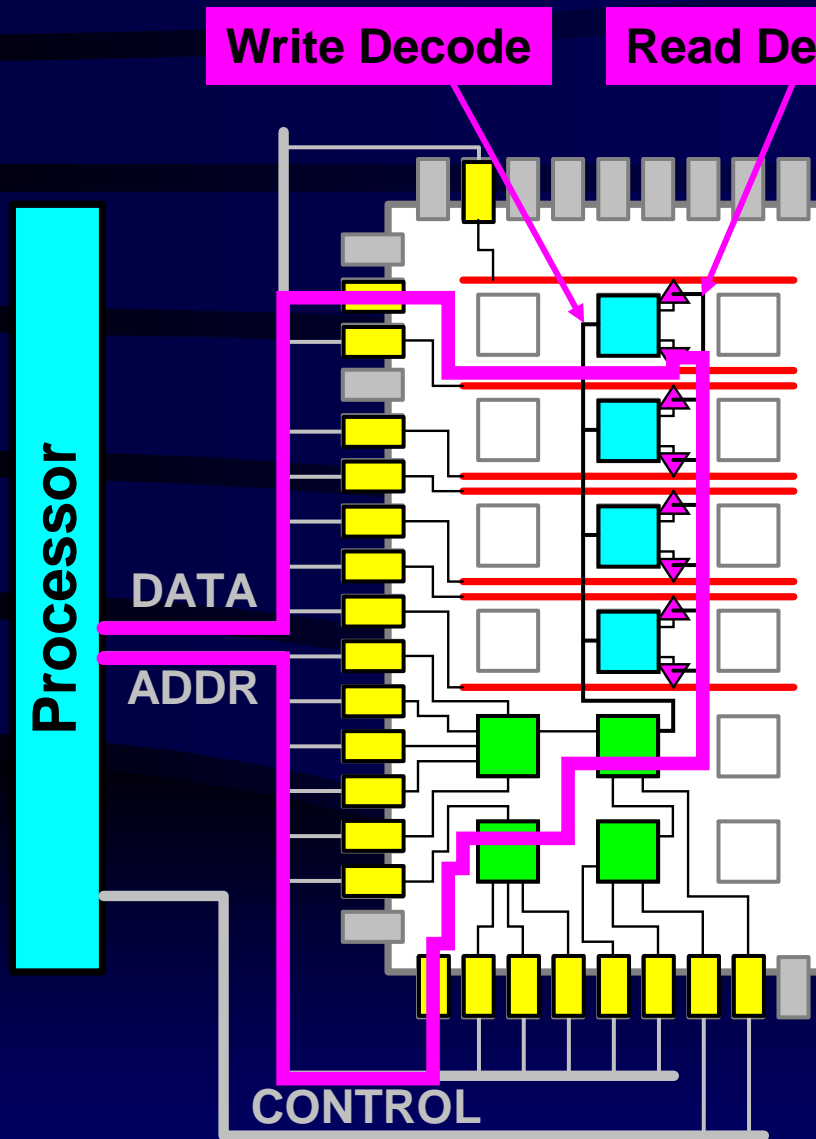


# Configurable System-on-Chip Technical Challenges

- Communication between the system and programmable logic functions
  - Connecting to the data and address bus
  - Decoding/controlling bus transactions
  - Register intimacy
  - Debugging a system with both processor and programmable logic
- Maintain standard development flows
  - Leverage available compilers, debuggers
  - Leverage existing logic design tools



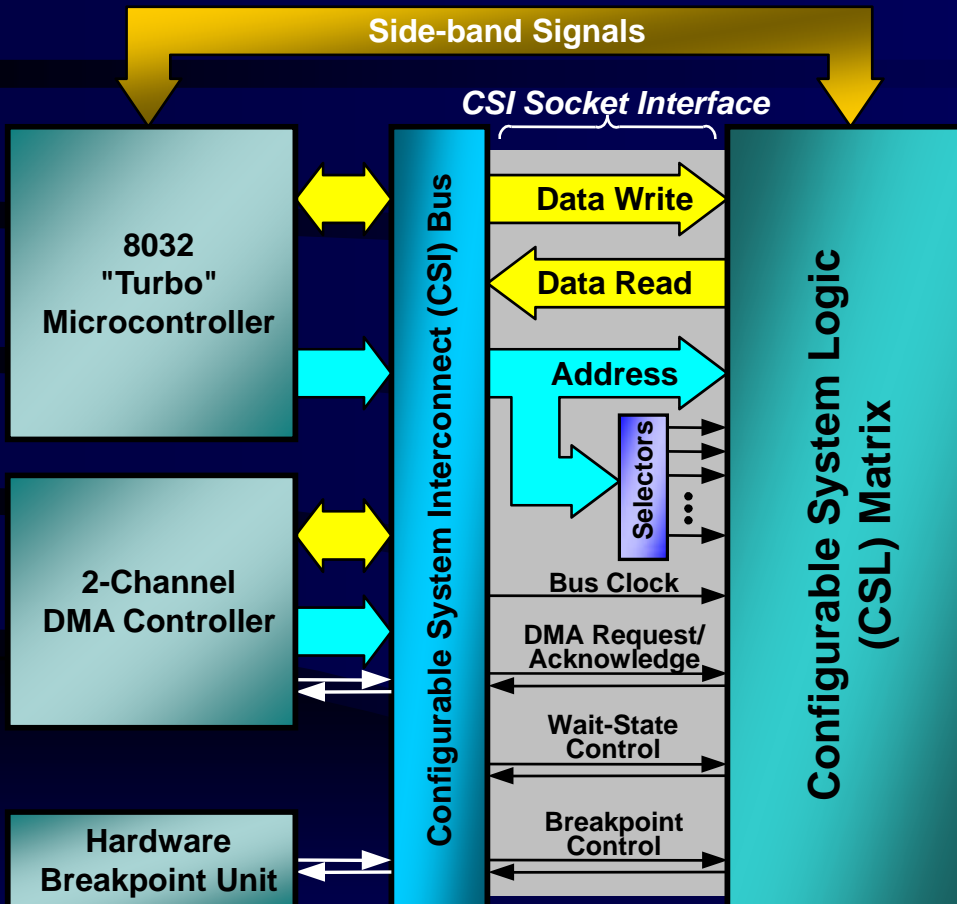
# Two-Chip Solution: CPU+FPGA/ASIC



- **I/Os between devices**
  - Many pins required, even for basic 8-bit interface
  - Adds delay to critical path
  - Extra power consumption and EMI in two-chip solution
- **Distributing address/data on-chip**
  - Uses programmable interconnect
  - Adds delay to critical path
  - Variable delays in some architectures
  - Some devices provide bidirectional bussing

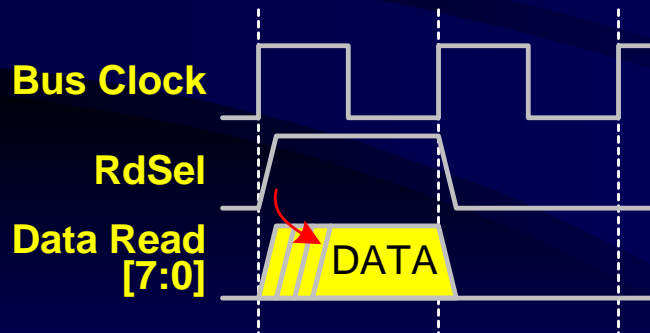
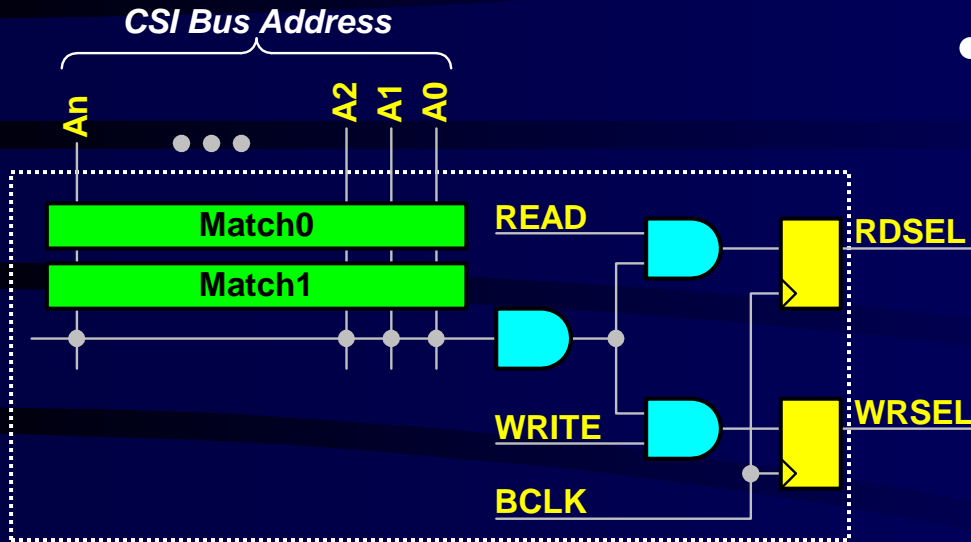
# Triscend Approach: CSI Bus Socket

(Configurable System Interconnect)



- Distributes bus signals to embedded program-mable logic
- No I/O required
- Predictable, synchronous timing
- Forward compatible with future device families
- Contention-free bussing
- Wait-state control
- DMA access
- Integrated debugging

# Selector



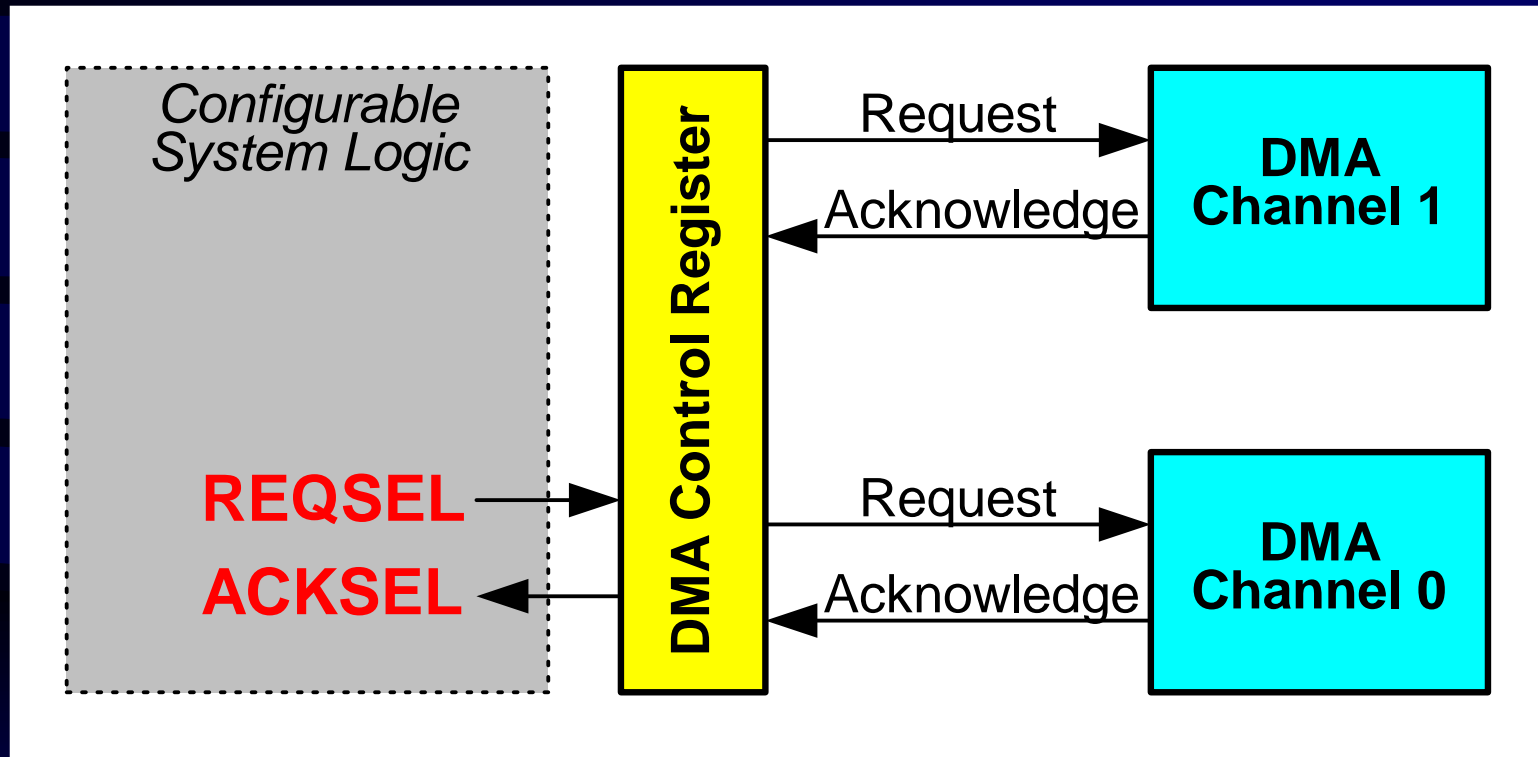
- Decode delay is constant (less than 5 ns after clock)

- **Fast address decoding**

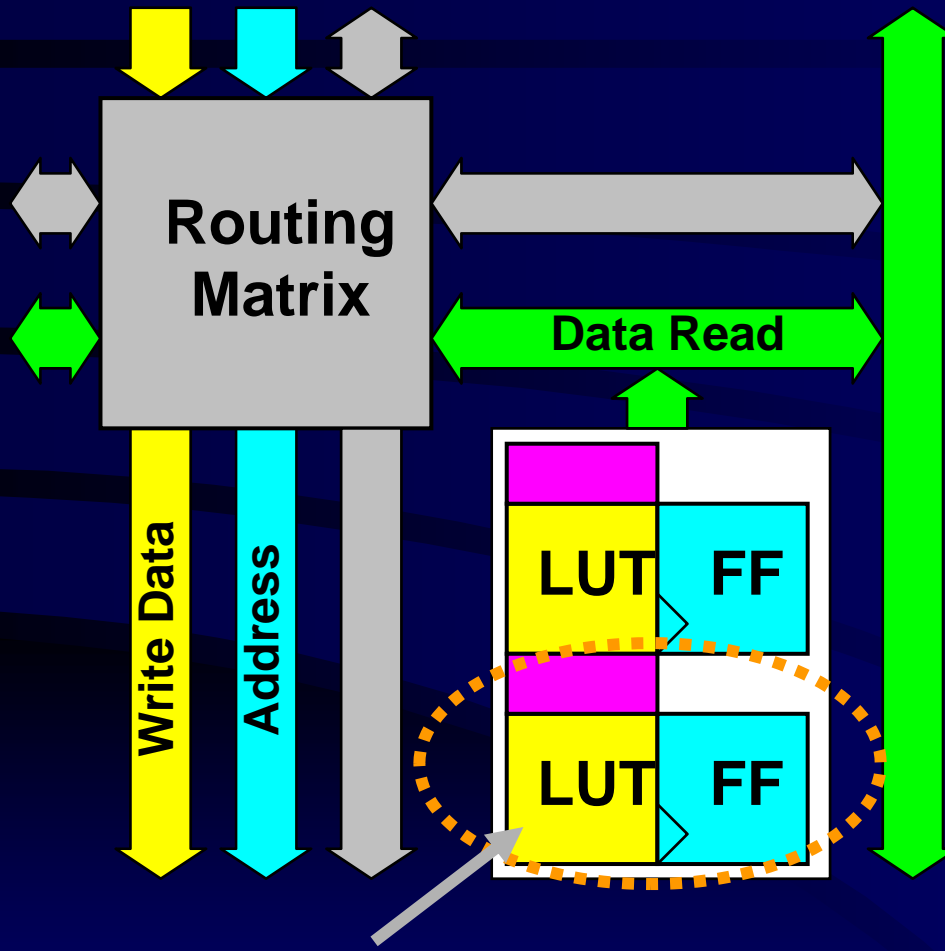
- Any address range
- Access type
  - Code
  - Data
  - **Special Function Register (SFR)**

Device	Selectors
TE502	16
TE505	32
TE512	72
TE520	128
TE532	200

# DMA Control Register (alternate Selector function)



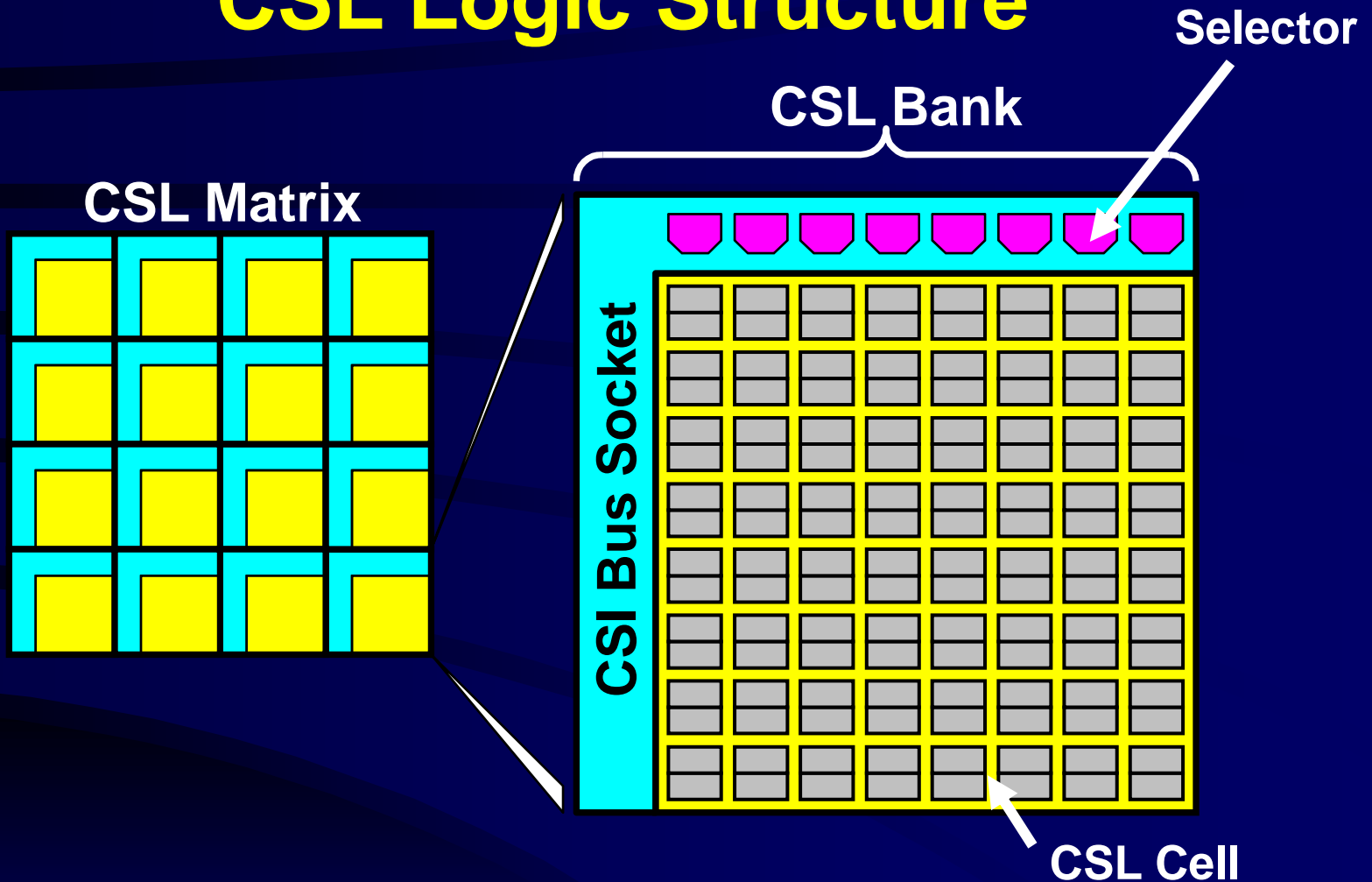
# CSL Cell Structure



CSL Cell = LUT+FF

- CSL cell perform various functions
  - Logic
  - Arithmetic
  - Memory
  - Bus
  - Sequential
- Intimate connection to the CSI system bus

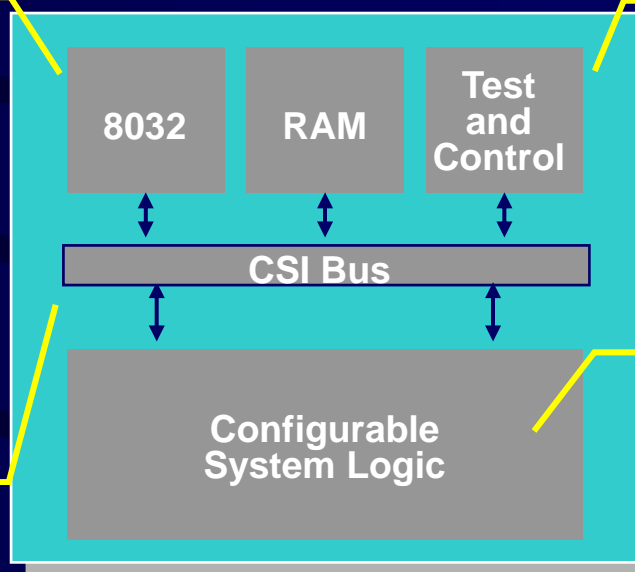
# CSL Logic Structure



- **CSL** = Configurable System Logic
- **CSI** = Configurable System Interconnect

# Configurable System-on-Chip Debugging Capabilities

Access to all address mapped and other key processor resources

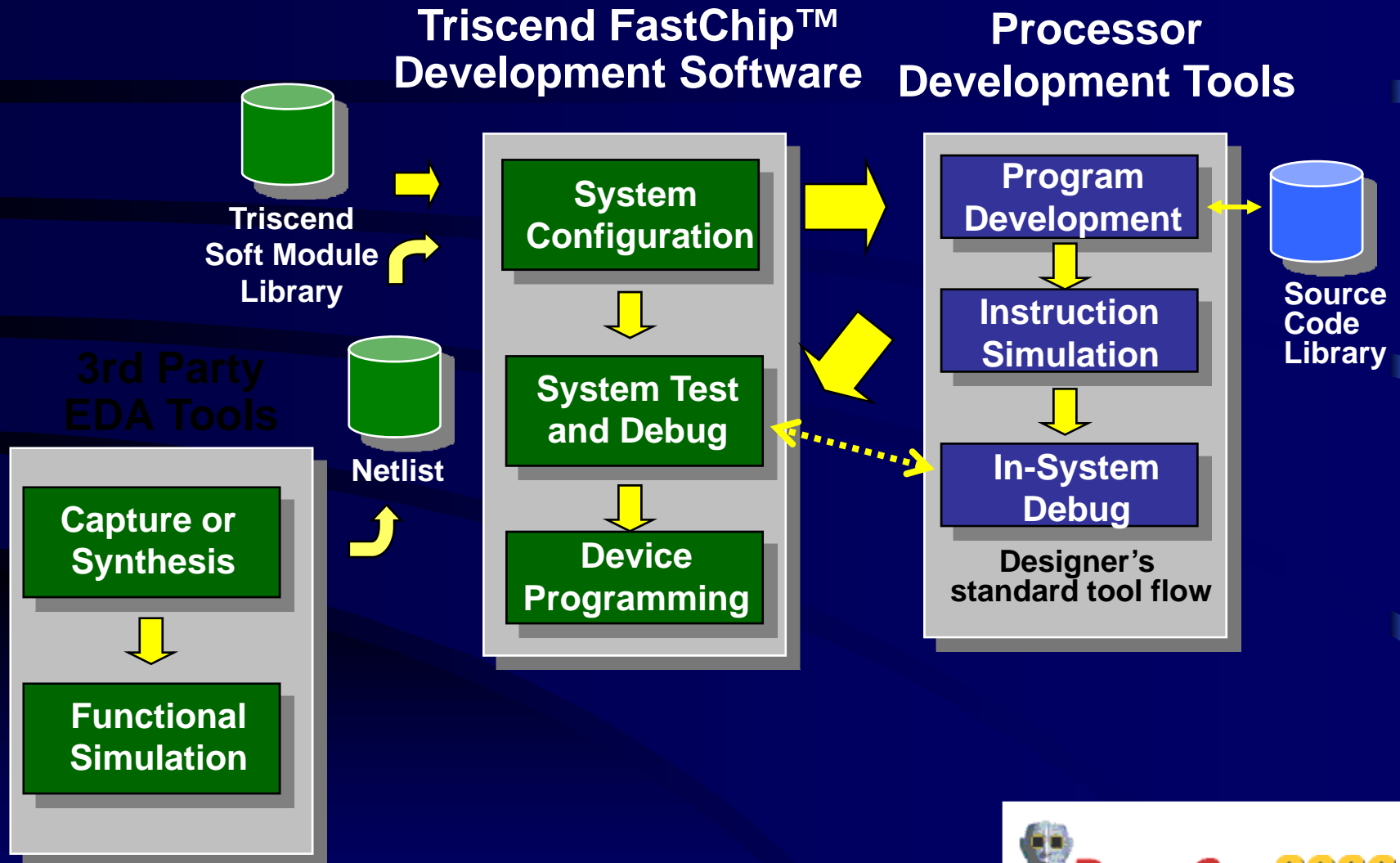


Commands from 3rd party debuggers translated to JTAG instructions

Breakpoint unit snoops the internal bus, providing complex runtime control features

All sequential and combinatorial logic nodes have complete observability

# Triscend CSoC Design Flow





# FastChip Development System

The screenshot displays the Triscend FastChip DesignExample software interface. The window title is "Triscend FastChip: DesignExample (Target Device: TE520S32-40Q) (Preview Release)". The interface includes a menu bar (File, Edit, View, Tools, Personalize, Help) and a toolbar with icons for Library, Import EDIF, I/O Editor, Generate, Bind, Download, Debug, and Stop.

On the left, the "Triscend Library" is expanded to show categories like 8032 Peripheral, Imported, Peripherals, Logic Modules, Compare, Arithmetic, I/O, and Primitives. A yellow callout bubble labeled "Soft Module Library" points to this library pane.

The main workspace is divided into several sections:

- Dedicated Resources:** A grid of hardware resources including Clocks, Timer\_1, UART, Watchdog, DMA 0, Power, Timer\_0, Timer\_2, Interrupts, Sideband, DMA 1, MIU, and 8032 MCU. A yellow callout bubble labeled "Dedicated Resources" points to this section.
- Configurable System Interconnect (CSI) Bus:** A central horizontal bar representing the system bus.
- Configurable System Logic:** A grid of logic modules including 24BitCntnr, CaptureMid, CounterCtrl, 7seg\_A, CaptureLow, CaptureHi, SevenSegment, and 7seg\_B. A yellow callout bubble labeled "Soft peripherals dragged into CSL matrix" points to this section.
- Programmable I/O Pins:** A grid of I/O components including DebugCounter, ReadSwitch, Display\_A, Display\_B, CaptureStrap, and CounterCl.

At the bottom, the "Resources Used" section shows usage statistics: CSI Selectors: 18/128 (14%), I/O Pins: 40/125 (32%), CSL Cells: 121/2048 (5%), and Performance: 40 MHz. A yellow callout bubble labeled "Resources Used Indicators" points to these statistics.

# Summary

- **Advanced process technologies enable Configurable System-on-Chip devices**
- **High-density, cost-effective, and flexible**
- **Ideal for fast time-to-market for embedded systems applications**
- **On-chip communication, development flow, and debugging were top development challenges**
- **More to come ...**

# For More Information



The image shows a screenshot of the Triscend website. The background is a blue sky with a person in a white shirt and tie looking up. A curved blue line on the left side contains navigation links: About Triscend, Products, Sales and Support, Learning Center, Contact Us, and Site Map. In the center, the text 'The Configurable Processor' is displayed above a small image of a processor chip. To the right of the chip, four lines point to the following features: Industry Standard Processor, Programmable Logic, Dedicated Bus, and Memory. The Triscend logo is in the top right corner. Below the chip, there is a 'What's New' section with two bullet points: 'Announcing the Triscend Configurable Processor' and 'Visit Triscend at the Embedded Systems Conference 11/3-11/5 in San Jose'.

**Triscend**

*The Configurable Processor*

Industry Standard Processor  
Programmable Logic  
Dedicated Bus  
Memory

**What's New**

- Announcing the Triscend Configurable Processor
- Visit Triscend at the Embedded Systems Conference 11/3-11/5 in San Jose

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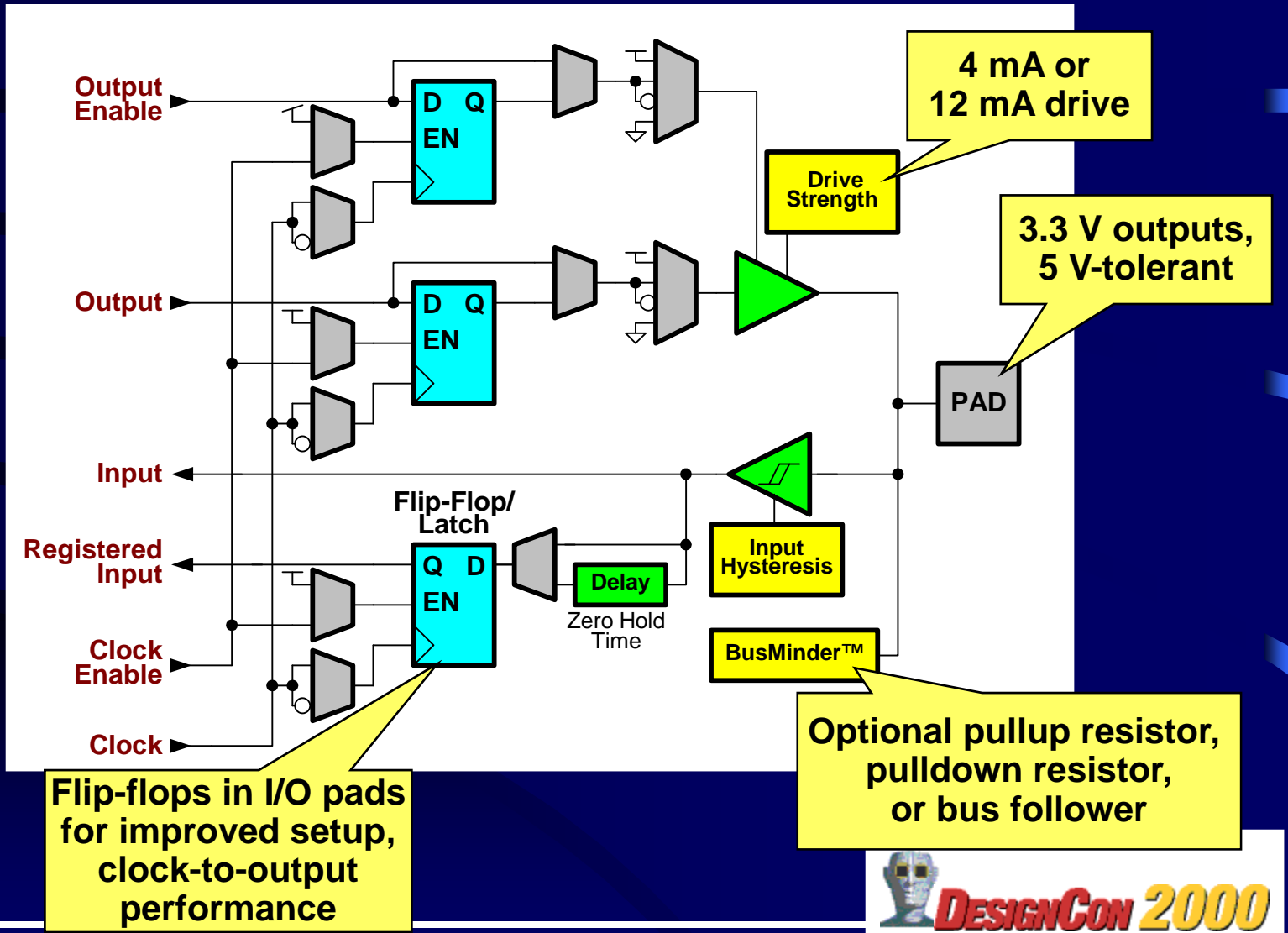
[www.triscend.com](http://www.triscend.com)



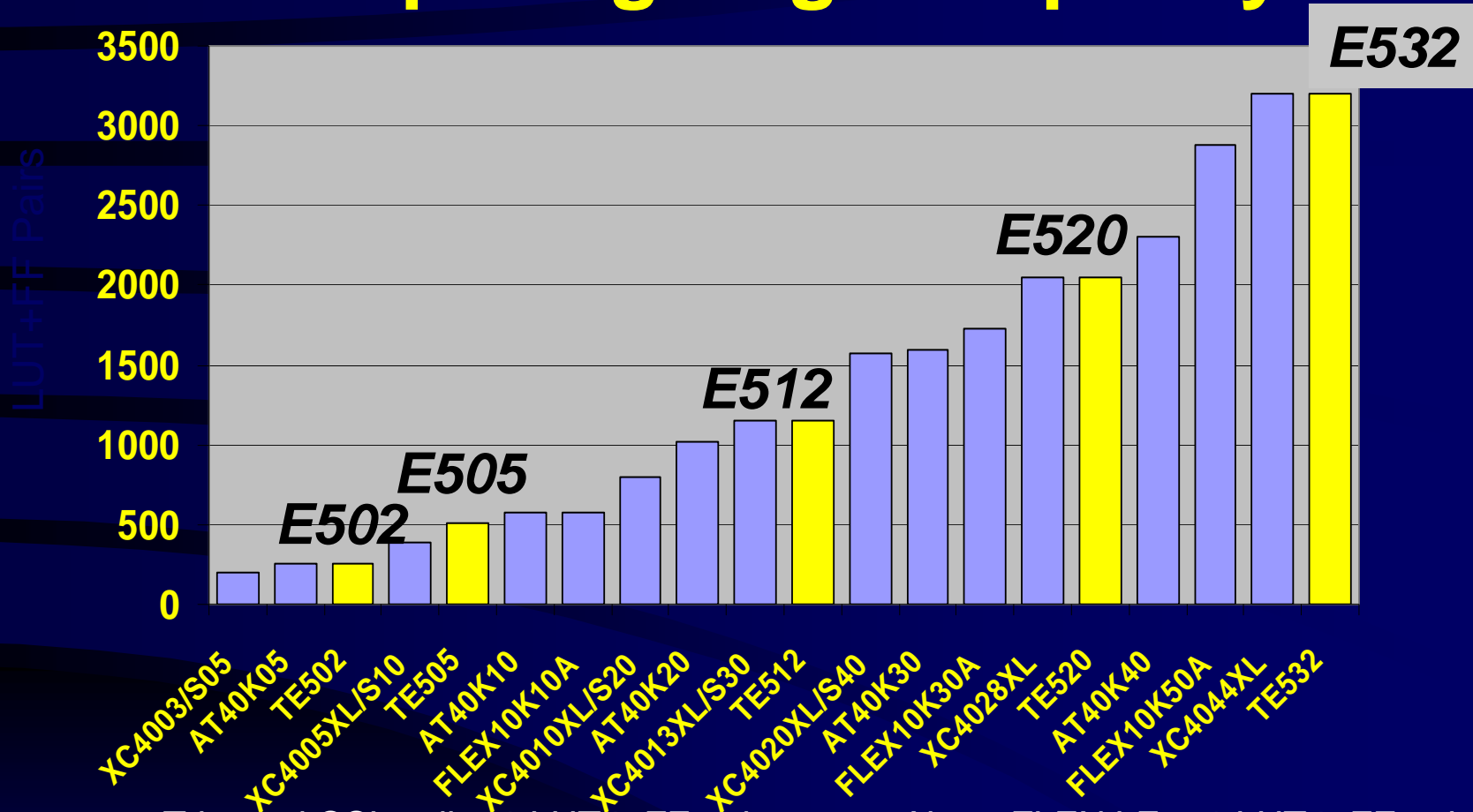
# Comparing 8052-class MCUs

Feature	Average 8052	Dallas 80C320	Philips XA-GA	Triscend E5
8051/8052 binary compatible	Yes	Yes	No	Yes
Max. Frequency	24 MHz	33 MHz	30 MHz	40 MHz
Instruction cycle (clocks)	12	4	3	4
16-bit Timer/Counters	3	3	3	3+
Watchdog Timer	N/A	Yes	Yes	Yes
UARTs	1	2	2	1+
Interrupts	7	13	38	12+
Data Pointers	1	2	-	2
Wait-state support	N/A	N/A	Yes	Yes
PIO pins	32	32	32	60 to 316
On-chip internal RAM	256	256	512	256
On-chip MOVX RAM	N/A	N/A	N/A	8K to 64K
Glue-less memory interface	N/A	N/A	N/A	Yes
DMA channels	N/A	N/A	N/A	2
Maximum address space	64K	64K	1M/16M	64K/16M
On-chip debug hardware	N/A	N/A	Yes	Yes

# Programmable I/O (PIO)



# Comparing Logic Capacity



- Triscend CSL cell = 1 LUT4+FF pair
- Xilinx CLB = 2 LUT4+FF pair

- Altera FLEX LE = 1 LUT4+FF pair
- Atmel logic cell = 1 LUT4+FF pair